



UNITED STATES PATENT AND TRADEMARK OFFICE

cen

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,759	10/19/2004	Kari Pajukoski	60091.00345	4940
32294	7590	09/10/2007		
SQUIRE, SANDERS & DEMPSEY L.L.P. 14TH FLOOR 8000 TOWERS CRESCENT TYSONS CORNER, VA 22182			EXAMINER NGUYEN, LEON VIET Q	
			ART UNIT 2611	PAPER NUMBER
			MAIL DATE 09/10/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/511,759	Applicant(s) PAJUKOSKI, KARI	
	Examiner Leon-Viet Q. Nguyen	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 July 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 19-21, 29-34 and 36-38 is/are allowed.
- 6) ☒ Claim(s) 1-18, 22-28, 35 is/are rejected.
- 7) ☒ Claim(s) 12 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 October 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. This office action is in response to communication filed on 7/9/07. Claims 1-38 are pending on this application.

2. Applicant's amendment overcomes the following objection/rejection:

- a. Objection of claim 21.
- b. Rejection of claims 1-2, 4-7, 11 and 35 under 35 USC 102(e)
- c. Rejection of claims 3, 8-10, 12-34, and 36-38 under 35 USC 103(a)

1. Applicant's arguments, see Remarks, filed 7/9/07, with respect to the rejection(s) of claim(s) 1-38 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Matsuoka et al (US6418173), Shearer, III (US20030063682), Uta et al (US6144694), Piirainen et al (US20030219079A1), Pierzga et al (US20020114270A1), Currivan et al (US7110434), Zehavi (US5602833) and Billsberry (US20030001669).

Response to Remarks

Regarding claims 1, 2, and 35 applicant argues that Matsuoka fails to teach or suggest determining an error signal using the transmissible signal and the limiting signal (Remarks page 17).

Examiner respectfully disagrees.

As stated in the previous office action, the distortion compensating section 107 in figure 1 calculates a distortion compensation signal 119. The distortion signal is based on amplitude limiting signal 116. Furthermore amplitude limiting signal 116 is obtained from transmission signal 113 (see col. 5 lines 13-16). Therefore it is interpreted that the distortion compensation signal is generated from the limiting signal 116 and indirectly generated from transmission signal.

Applicant also argues that the distortion compensating section 107 in Matsuoka does not teach generating an error signal (Remarks page 18).

Examiner respectfully disagrees.

Distortion compensation section 107 in figure 1 generates a distortion compensation signal 119. Although the signal is not explicitly an error signal, it is well known in the art that distortion is synonymous with error. Therefore it is interpreted that distortion compensation signal is the same as an error signal.

Applicant further argues that Matsuoka fails to teach or suggest generating a limited transmissible signal by reducing an error signal filtered using

Art Unit: 2611

a filter matched to a chip pulse waveform from the transmissible signal (Remarks page 18).

Examiner respectfully disagrees.

A filter matched to a chip pulse waveform is merely a pulse shaping filter. Amplitude pulse shaping filters are well known in the art to limit the amplitude of baseband signals. The distortion components are interpreted to limit the amplitude (col. 6 lines 10-11), which is the same function as an amplitude pulse shaping filter. The distortion components include the distortion compensation signal which is interpreted as the error signal and has a limited or reduced amplitude. Therefore examiner asserts that the distortion component is the same as a filter matched to a chip pulse waveform. Furthermore, it is not specified what the chip pulse waveform is in particular.

Regarding claim 3, applicant argues that Uta does not teach or suggest determining a limiting signal from the combination signal (Remarks page 23).

Examiner respectfully disagrees.

It is well known in the art that multiplexing signals is used in wireless communications to increase bandwidth. Therefore multiplexing of two signals modulated on different carriers to a combination signal, as taught by Uta, would be beneficial if used in lieu of the limiting signal 116 in fig. 1 of Matsuoka. The combination of Matsuoka and Uta would teach the limitation as claimed.

Art Unit: 2611

Applicant further argues that Matsuoka and Uta fail to teach or suggest generating limited transmissible signals by reducing each error signal part filtered using the filter matched to a chip pulse waveform from a corresponding transmissible signal." (Remarks page 24)

Examiner respectfully disagrees.

See the response above to the arguments with respect to claims 1 and 2.

Regarding claim 13, applicant argues the combination of Currivan and Matsuoka fail to disclose or suggest all of the elements of claims 2 and 13, in particular "determining an error signal using the transmissible signal and the limiting signal; and generating a limited transmissible signal by reducing an error signal filtered using the filter matched to a chip pulse waveform from the transmissible signal" (Remarks page 31).

Examiner respectfully disagrees.

The point has been addressed above in reference to claim 2. Furthermore the argument is moot in view of the new grounds of rejection.

Regarding claim 14, applicant argues the combination of Zehavi and Matsuoka fail to disclose or suggest all of the elements of claims 2 and 14, in particular "determining an error signal using the transmissible signal and the limiting signal; and generating a limited transmissible signal by reducing an error

Art Unit: 2611

signal filtered using the filter matched to a chip pulse waveform from the transmissible signal" (Remarks page 32-33).

Examiner respectfully disagrees.

The point has been addressed above in reference to claim 2. Furthermore the argument is moot in view of the new grounds of rejection.

Regarding claims 16-17, applicant argues that Billsberry is silent as to teaching or suggesting "combining at least two signals modulated on different carriers to a combination signal; determining a limiting signal from the combination signal filtered using a pulse shaping filter...and generating limited transmissible signals by reducing each error signal part filtered using the filter matched to a chip pulse waveform from a corresponding transmissible signal." (Remarks page 34).

Examiner agrees, however the argument has been addressed with respect to response to claim 3.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1-2, 4-7, 11, 22-25, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173) in view of Shearer, III (US20030063682).

Re claim 1, Matsuoka teaches a method for limiting a signal in a transmitter (col. 2 lines 31-34) at chip level, the method comprising:

determining a limiting signal (115, 116) from a transmissible signal (113, col. 5 lines 5-7) filtered using a pulse shaping filter (103), and

determining an error signal (the output 119 from 107) using the transmissible signal (113) and the limiting signal (115, 116).

Matsuoka fails to teach generating a limited transmissible signal by reducing an error signal filtered using the filter matched to a chip pulse waveform from the transmissible signal. However Shearer III teaches using a pulse-shaping filter to shape and spread information conveyed in each interval of modulated data (§10002). Furthermore, it is well known in the art that filters reduce the amplitude of a signal.

Therefore taking the combined teachings of Matsuoka and Shearer III as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the pulse shaping of Shearer into the method of Matsuoka. The motivation to combine Shearer and Matsuoka would be to permit efficient recovery of information without significant intersymbol interference (§10002).

Re claim 2, Matsuoka teaches a method for limiting a signal in a transmitter (col. 2 lines 31-34) at chip level, the method comprising:

determining a limiting signal (115 and 116 in fig. 3) from a transmissible signal (113 in fig. 3, col. 5 lines 5-7) filtered using a filter (103 in fig. 3),

determining an error signal (the output 119 from 107) using the transmissible signal (113 in fig. 3) and the limiting signal (115 and 116 in fig. 3),

orthogonalizing the error signal (108 in fig. 3) filtered using the filter matched to a chip pulse waveform (107 in fig. 3), and

generating a limited transmissible signal (122 in fig. 3) by reducing the orthogonalized error signal from the transmissible signal (col. 6 lines 10-11, the distortion components includes the distortion compensation signal which is interpreted as the error signal and has a limited or reduced amplitude).

Matsuoka fails to teach where the filter is a pulse shaping filter. However Shearer III teaches using a pulse-shaping filter to shape and spread information conveyed in each interval of modulated data (¶0002). Furthermore, it is well known in the art that filters reduce the amplitude of a signal.

Therefore taking the combined teachings of Matsuoka and Shearer III as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the pulse shaping of Shearer into the method of Matsuoka. The motivation to combine Shearer and Matsuoka would

Art Unit: 2611

be to permit efficient recovery of information without significant intersymbol interference (§0002).

Re claim 4, Matsuoka the modified invention of teaches a method wherein the transmissible signal is a baseband signal (abstract of Matsuoka, 113 in fig. 1 of Matsuoka).

Re claim 5, the modified invention of Matsuoka teaches a method wherein the limiting signal is a baseband signal (115 and 116 in fig. 1 of Matsuoka).

Re claim 6, the modified invention of Matsuoka teaches a method wherein the error signal is a baseband signal (119 in fig. 1 of Matsuoka, the I and Q signals of the distortion compensation signal).

Re claim 7, the modified invention of Matsuoka teaches a method wherein the limiting signal (115 and 116 in fig. 1 of Matsuoka) is determined by means of a threshold value set (102 in fig. 1 of Matsuoka) for the power or amplitude values (102 in fig. 1 of Matsuoka, col. 5 lines 5-12).

Art Unit: 2611

Re claim 11, the modified invention of Matsuoka teaches a method wherein a second clipping stage is added (105 in fig. 1 of Matsuoka).

Re claim 22, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 4.

Re claim 23, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 5.

Re claim 24, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 6.

Re claim 25, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 7.

Re claim 35, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 1.

Art Unit: 2611

3. Claim 3, 15, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173) in view of Uta et al (US6144694) and further in view of Shearer, III (US20030063682).

Re claim 3, Matsuoka teaches a method for limiting a signal in a transmitter (col. 2 lines 31-34) at chip level, the method comprising:

determining a limiting signal (115 and 116 in fig. 3) from the combination signal (113 in fig. 3) filtered using a filter (103 in fig. 3),

determining an error signal (the output 119 from 107 in fig. 3) using the combination signal (113 in fig. 3) and the limiting signal (115 and 116 in fig. 3),

dividing the error signal onto different carriers in a predetermined manner (col. 5 lines 33-36),

However Matsuoka fails to teach combining at least two signals modulated on different carriers to a combination signal. Uta teaches combining n different channels into a single multiplexed channel (fig. 8, 11-1 and 11-2 combined in 18).

Therefore taking the combined teachings of Matsuoka and Uta as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the combination method of Uta into the transmitter of Matsuoka to provide a signal that is similar to white noise so that the signals of all channels have less chance of having the same value simultaneously (col. 1 lines 51-57) and reduce transmission back-off without creating a spurious (col. 2 lines 15-19).

Matsuoka also fails to teach generating limited transmissible signals by reducing each error signal part filtered using the filter matched to a chip pulse waveform from a corresponding transmissible signal. However Shearer III teaches using a pulse-shaping filter to shape and spread information conveyed in each interval of modulated data (§0002). Furthermore, it is well known in the art that filters reduce the amplitude of a signal.

Therefore taking the combined teachings of Matsuoka and Shearer III as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the pulse shaping of Shearer into the method of Matsuoka. The motivation to combine Shearer and Matsuoka would be to permit efficient recovery of information without significant intersymbol interference (§0002).

Re claim 15, the modified invention of Matsuoka teaches a method wherein the orthogonalization of the error signal (108 in fig. 3 of Matsuoka) is carried out according to carriers (col. 5 lines 33-36 of Matsuoka).

Re claim 18, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 1. It is implied and necessary to have a transmitter to perform the method as claimed. Furthermore,

Art Unit: 2611

Uta teaches the means for filtering the limited transmissible signals using the pulse-shaping filter (fig. 4, 24a).

Therefore taking the combined teachings of Matsuoka, Shearer and Uta as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the combination method of Uta into the transmitter of Matsuoka and Shearer. The motivation to combine Matsuoka, Shearer, and Uta would be to limit the bandwidth of an over-sampled signal (col. 1 lines 44-45). It would be obvious to one of ordinary skill in the art that limiting the bandwidth also reduces the unwanted noise.

4. Claims 8-9 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173) and Shearer, III (US20030063682) and further in view of Piirainen et al (US20030219079A1).

Re claim 8, the modified invention of Matsuoka teaches a method wherein the limiting signal (115 and 116 in fig. 1 of Matsuoka) is determined by means of a threshold value set (102 in fig. 1 of Matsuoka) for the power or amplitude values (102 in fig. 1 of Matsuoka, col. 5 lines 5-12 of Matsuoka). However Matsuoka fails to teach the threshold value being set bearing in mind the maximum value predetermined for an error vector magnitude.

Piirainen teaches considering the allowed maximum value of the error vector magnitude, or EVM, when determining a threshold value (¶0031).

Therefore taking the modified teachings of Matsuoka and Shearer with Piirainen as a whole, it would have been obvious to one of ordinary skill in the art

Art Unit: 2611

at the time the invention was made to incorporate the method of taking the EVM into consideration when formulating threshold values into the transmitter of Matsuoka and Shearer. The motivation to combine Matsuoka, Shearer, and Piirainen would be to improve the quality of modulation (§0034).

Re claim 9, the modified invention of Matsuoka teaches a method wherein the limiting signal (115 and 116 in fig. 1 of Matsuoka) is determined by means of a threshold value set (102 in fig. 1 of Matsuoka) for the power or amplitude values (102 in fig. 1 of Matsuoka, col. 5 lines 5-12 of Matsuoka). However Matsuoka fails to teach the threshold value being set bearing in mind the maximum value predetermined for a peak code domain error.

Piirainen teaches considering the maximum value of the peak code domain error used in WDMA systems when determining a threshold value (§0031).

Therefore taking the modified teachings of Matsuoka and Shearer with Piirainen as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of taking the peak code domain error into consideration when formulating threshold values into the transmitter of Matsuoka and Shearer. The motivation to combine Matsuoka, Shearer, and Piirainen would be to determine if there is an error in the composed signal resulting from inaccurate modulation (§0031).

Art Unit: 2611

Re claim 26, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 8.

Re claim 27, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 9.

5. Claims 10 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173) and Shearer, III (US20030063682) and further in view of Pierzga et al (US20020114270A1).

Re claim 10, the modified invention of Matsuoka teaches a method wherein the limiting signal (115 and 116 in fig. 1 of Matsuoka) is determined by means of a threshold value set (102 in fig. 1 of Matsuoka) for the power or amplitude values (102 in fig. 1 of Matsuoka, col. 5 lines 5-12 in Matsuoka). However Matsuoka fails to teach the threshold value being set so as to obtain the desired Peak-to-Mean Ratio, Peak-to-Average Ratio, Crest factor of the power or amplitude.

Pierzga teaches the use of a peak-to-mean reduction circuit (132 in fig. 14) to detect whether any samples within a signal period are in excess of a predetermined threshold (¶0144).

Therefore taking the modified teachings of Matsuoka and Shearer with Pierzga as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the reduction circuit of Pierzga into the transmitter of Matsuoka and Shearer. The motivation to combine

Art Unit: 2611

Matsuoka, Shearer, and Pierzga would be to alleviate the problem of distortion and intermodulation (§0144). Furthermore, it is well known in the art that the peak-to-mean ratio, peak-to-average ratio, and crest factor are inter-related and it would have been obvious and necessitated to use the reduction circuit to reduce the peak-to-average ratio and crest factor.

Re claim 28, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 10.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173) and Shearer, III (US20030063682) and further in view of Currivan et al (US7110434).

Re claim 13, the modified invention of Matsuoka fails to teach a method wherein unused codes are utilized in orthogonalization. However Currivan teaches using a linear combination of unused codes to cancel interference (col. 2 lines 31-33), those being orthogonal codes (col. 19 lines 56-58). It is well known in the art that orthogonal transformation is used to facilitate interference cancellation (col. 24 lines 9-14).

Therefore taking the modified teachings of Matsuoka and Shearer with Currivan as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of unused codes as taught by Currivan into the transmitter of Matsuoka and Shearer. The motivation

to combine Matsuoka, Shearer, and Currivan would be to cancel interference (col. 2 lines 31-33).

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173) and Shearer, III (US20030063682) and further in view of Zehavi (US5602833).

Re claim 14, the modified invention of Matsuoka fails to teach a method wherein codes used at a lower modulation level are utilized in orthogonalization. However Zehavi teaches using lower order modulation values of M (col. 18 lines 19-26) to be used in orthogonal functions (col. 18 lines 27-31).

Therefore taking the modified teachings of Matsuoka and Shearer with Zehavi as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of using lower modulation values of Zehavi into the transmitter of Matsuoka and Shearer. The motivation to combine Matsuoka, Shearer, and Zehavi would be to increase the energy of modulation symbols (col. 18 lines 15-17) and save memory space by re-using codes.

8. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173), Uta et al (US6144694) and Shearer, III (US20030063682) and further in view of Billsberry (US20030001669).

Re claim 16, the modified invention of Matsuoka fails to teach a method

Art Unit: 2611

wherein the error signal is divided equally between different carriers. However Billsberry teaches the use of an error signal splitter to divide an error signal output into equal strength portions (§0027).

Therefore taking the modified teachings of Matsuoka, Uta, and Shearer with Billsberry as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the error signal splitter of Billsberry into the transmitter of Matsuoka, Uta, and Shearer. The motivation to combine Matsuoka, Uta, Shearer, and Billsberry would be to cancel distortion in the signal at the RF output (§0027).

Re claim 17, the modified invention of Matsuoka fails to teach a method wherein the error signal is divided between different carriers in relation to the power or amplitude values to be clipped. However Billsberry teaches an error splitter that apportions an error signal according to the magnitudes of the signals input into the splitter (§0027).

Therefore taking the modified teachings of Matsuoka, Uta, and Shearer with Billsberry as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the error signal splitter of Billsberry into the transmitter of Matsuoka, Uta, and Shearer. The motivation to combine Matsuoka, Uta, Shearer, and Billsberry would be to cancel distortion in the signal at the RF output (§0027).

Allowable Subject Matter

9. Claims 19-21, 29-34, and 36-38 are allowed.
10. The following is a statement of reasons for the indication of allowable subject matter: The allowable subject matter in independent claims 19-21 and 36-38 pertain to means for determining a first limiting signal from a transmissible signal filtered using a pulse shaping filter, means for determining a first error signal using the transmissible signal and the first limiting signal, means for orthogonalizing the first error signal filtered using the filter matched to a chip pulse waveform, means for generating a first limited transmissible signal by reducing the orthogonalized first error signal from the transmissible signal, means for determining a second limiting signal from the first limited transmissible signal filtered using the pulse shaping filter, means for determining a second error signal using the first limited transmissible signal and the second limiting signal, means for generating a second limited transmissible signal by reducing the second error signal filtered using the filter matched to a chip pulse waveform from the transmissible signal, means for filtering the second limited transmissible signal using the pulse shaping filter.
11. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Art Unit: 2611

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon-Viet Q. Nguyen whose telephone number is 571-270-1185. The examiner can normally be reached on monday-friday, alternate friday off, 7:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leon-Viet Nguyen/
Assistant Examiner Art Unit 2611


DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER